

Claims

- [c1] 1.A method for allocating memory bandwidth comprising:
assigning a fixed priority of access to memory bandwidth to one or more direct memory access (DMA) machines; and
assigning a programmable priority of access to memory bandwidth to a processing unit;
wherein the programmable priority of the processing unit allows priority allocation between the one or more DMA machines and the processing unit to be adjusted dynamically.
- [c2] 2.The method of claim 1 wherein assigning a fixed priority to the one or more DMA machines includes assigning a fixed priority to one or more DMA channels, the one or more DMA channels corresponding to the one or more DMA machines.
- [c3] 3.The method of claim 2 wherein the programmable priority of the processing unit allows priority allocation between the one or more DMA channels and the processing unit to be adjusted dynamically.

- [c4] 4.The method of claim 1 wherein assigning a fixed priority to one or more DMA machines includes assigning a different fixed priority to each of the one or more DMA machines.
- [c5] 5.The method of claim 4 wherein assigning a programmable priority to the processing unit includes assigning one of a plurality of programmable processing unit priorities to the processing unit, the plurality of programmable processing unit priorities being interleaved with the different fixed priorities of the one or more DMA machines.
- [c6] 6.The method of claim 4 further comprising delaying access to memory bandwidth for the one or more DMA machines having a lower priority than the processing unit.
- [c7] 7.The method of claim 1 wherein assigning the fixed priority to one or more DMA machines includes assigning the fixed priority to a task to be performed by the one or more DMA machines; and wherein assigning the programmable priority to a processing unit includes assigning the programmable priority to a task to be performed by the processing unit.
- [c8] 8.The method of claim 7 further comprising allocating

memory bandwidth to the task of the one or more DMA machines and the task of the processing unit having the highest priority.

- [c9] 9.The method of claim 8 further comprising adjusting the priority of the processing unit.
- [c10] 10.The method of claim 1 further comprising delaying access to memory bandwidth for the one or more DMA machines having a lower priority than the processing unit.
- [c11] 11.The method of claim 1 further comprising allocating memory bandwidth to a task to be performed by one of the one or more DMA machines and the processing unit of a highest priority.
- [c12] 12.The method of claim 11 further comprising adjusting the priority of the processing unit.
- [c13] 13.An apparatus for allocating memory bandwidth comprising:
 - a processing unit adapted to execute tasks;
 - one or more direct memory access (DMA) machines each responsible for retrieving data and providing the retrieved data to the processing unit;
 - a bus, coupled to the processing unit and the one or more DMA machines, and adapted to provide communi-

cation between each of the one or more DMA machines, the processing unit and a data resource; and
a dynamic priority allocation circuit adapted to allocate priority of access to the data resource between each of the one or more DMA machines and the processing unit.

[c14] 14.The apparatus of claim 13 further comprising a register coupled to the dynamic priority allocation circuit, and adapted to store the priority of the processing unit.

[c15] 15.The apparatus of claim 13 wherein the dynamic priority allocation circuit is adapted to:
assign a fixed priority to the one or more DMA machines;
and
assign a programmable priority to the processing unit;
wherein the programmable priority of the processing unit allows priority allocation between the one or more DMA machines and the processing unit to be adjusted dynamically.

[c16] 16.The apparatus of claim 15 wherein the dynamic priority allocation circuit is further adapted to assign a fixed priority to one or more DMA channels, the one or more DMA channels corresponding to the one or more DMA machines.

[c17] 17.The apparatus of claim 15 wherein the dynamic pri-

ority allocation circuit is further adapted to assign a different fixed priority to each of the one or more DMA machines.

[c18] 18.The apparatus of claim 17 wherein the dynamic priority allocation circuit is further adapted to assign one of a plurality of programmable processing unit priorities to the processing unit, the plurality of programmable processing unit priorities being interleaved with the different fixed priorities of the one or more DMA machines.

[c19] 19.The apparatus of claim 17 wherein the dynamic priority allocation circuit is further adapted to delay access to memory bandwidth for the one or more DMA machines having a priority lower than the processing unit.

[c20] 20.The apparatus of claim 15 wherein the dynamic priority allocation circuit is further adapted to assign the fixed priority to a task to be performed by the one or more DMA machines; and
assign the programmable priority to a task to be performed by the processing unit.

[c21] 21.The apparatus of claim 20 wherein the dynamic priority allocation circuit is further adapted to allocate memory bandwidth to the task of the one or more DMA machines and the task of the processing unit having the

highest priority.

- [c22] 22.The apparatus of claim 21 wherein the dynamic priority allocation circuit is further adapted to adjust the priority of the processing unit.
- [c23] 23.The apparatus of claim 15 wherein the dynamic priority allocation circuit is further adapted to delay access to memory bandwidth for the one or more DMA machines having a priority lower than the processing unit.
- [c24] 24.The apparatus of claim 15 wherein the dynamic priority allocation circuit is further adapted to allocate memory bandwidth to a task to be performed by one of the one or more DMA machines and the processing unit of the highest priority.
- [c25] 25.The apparatus of claim 24 wherein the dynamic priority allocation circuit is further adapted to adjust the priority of the processing unit.